

July 28, 2004

ONE SHEET

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	High Voltage Circuits Implemented Using Low Voltage Transistors						
Application Number : 10/710,692							
Confirmation Number:							
First Named Applicant:	Sanish JACOB						
Attorney Docket Number:	TI-37611						
Art Unit:	2815						
Examiner:	SHINGLETON						
Search string:	(4704547).pn						
US Patent Documents							
Note: Applicant is not required to submit a paper copy of cited US Patent Documents							
init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
ms	1	4704547	1987-11-03	Kirsch			
Signature							
Examiner Name				Date			
SHINGLETON				2/28/2007			

Please type a plus sign (+) inside this box

PTO/SB/08A (08-00)

Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet

1

of

2

Application Number

10/710,692

Filing Date

July 28, 2004

First Named Inventor

Sanish koshy jacob!

Group Art Unit

~~UNASSIGNED~~

Examiner Name

~~UNASSIGNED~~

Attorney Docket Number

TI-37611

U.S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]

Examiner Signature	SHINGLETON	Date Considered	2-28-68 8-2-67
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*EXAMINER: Initial reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.**

August 3, 2004
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two sheets

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Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Complete if Known			
		Application Number	10/710,692		
		Filing Date	July 28, 2004		
		First Named Inventor	Sanish koshy jacob		
		Group Art Unit	UNASSIGNED 2815		
		Examiner Name	UNASSIGNED SHINGLETON		
Sheet	2	of	2	Attorney Docket Number	TI-37611

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
MB		Hector Sanchez, Joshua Siegel, Carmine Nicoletta, James .p and Nissen ,jose Alvarez , "A Versatile 3.3/2.5/1.8-V CMOS I/O Driver Bulit in a 0.2-um ,3.5-nm Tox, 1.8-V CMOS Technology " in IEEE Journal of Solid State Circuits Vol 34. pp. 1501-1511, No.11, November 1999.	
MB		Changsik Yoo, Min -Kyu Kim , and Wonchan kim , " A Static Power Saving TTL-to -CMOS Input buffer " in IEEE Journal of Solid State Circuits. Vol 30, pp. 616- 620, No. 5, may 1995.	

Examiner Signature	SHINGLETON	Date Considered	2-28-07
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